

CURRENT MODE DELTA-SIGMA-MODULATION FOR LOW-VOLTAGE OPERATION

**Karsten Leitis,
Tommy Halim,**

University of Applied Sciences Gießen-Friedberg, Germany

Abstract

Delta-Sigma modulation is a widely spread technique for high accuracy analog to digital conversion. Mostly they operate voltage based. In this paper a method for Delta-Sigma modulation in current mode is presented. The method is optimized for low-voltage operation. The system consists of a current differential stage, a current based integrator, a clocked comparator, a current reference circuit and a current based DAC. The first order modulator operates at power supply voltage of 1.5 V and is being realized in a 0.35 μ CMOS technology.

Keywords: current mode delta-sigma modulation, low voltage

INTRODUCTION

Delta-Sigma converter is one of the most used analog-to-digital converter nowadays. It offers high performances in resolution and the system is quite easy to build. Mostly, delta-sigma converters available on the market are based on voltage mode techniques. In the last years, current mode circuit technique has been recognized as an interesting topic among the market. It has a big potential in a mixed analog digital design which is needed in a sensor system. The power consumption is an advantage as well. With current mode technique, the system can be made in a lower supply voltage.

There are growing demands on consumer electronics with progressively lower supply voltages. Mobile applications, for example, need a low-power circuitry to enable longer battery operation. One solution is by reducing the supply voltage. However the performance of the system cannot be compromised. Thus a circuit mode system is one of the promising solutions for this issue.

This paper presents a CMOS current-mode delta-sigma converter which can be operated with a 1.5V supply voltage. The system performances are evaluated by simulation. The system will be realized in 0.35 μ m technology.

SYSTEM ARCHITECTURE

Delta-Sigma modulators input stages are the differential input providing the delta function and an integrating circuitry performing the sigma function. For a current-mode Delta-Sigma modulator these circuits are created with basic current processing circuit elements. Figure 1 depicts all circuit blocks.

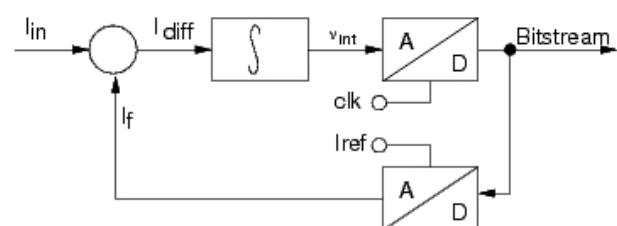


Fig. 1. System Architecture of
Current-mode Delta-Sigma Modulator

An input current I_{in} with the bandwidth BW subtracted by a feedback current I_f provide a differential current signal for the current integrator. The output voltage of the current integrator v_{int} delivers the signal for a voltage-mode A/D converter. For this first order modulator a one bit A/D converter – a comparator – is used. The output signal of the comparator is processed by a flip-flop operating with the clock signal clk . The over

Sampling rate OSR is given by:

$$OSR = \frac{f_c}{2 BW} \quad (1)$$

The output of the flip-flop is at the same time the output signal of the Delta-Sigma modulator – the bitstream.

The bitstream is also the input signal of the one bit current-mode based D/A converter. It controls the switching of the reference current I_f in the feedback loop.

An ideal n-bit Delta-Sigma modulator has a SNR given by equation 2,

$$SNR = 10 \log \left[\frac{3 \pi^2 V^2}{2} \cdot 2^{2K} \cdot OSR^2 \right] \quad (2)$$

where N is the number of quantizer bits and K the order of the modulator and OSR is the oversampling ratio.

CURRENT INTEGRATOR

The current integrator operates independently of reference currents. This is accomplished by the use of two current mirrors operating in a loop. The current integrator is shown in figure 2.

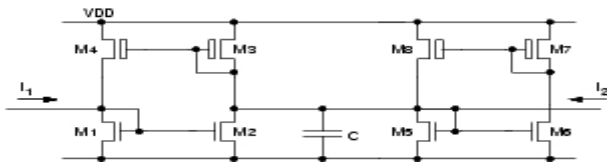


Fig. 2. Current Integrator

The current comparator operates at power supply voltage of $VDD_{min} = V_{gs} + V_{ds}$. It depends on the current adjusted how large V_{gs} is.

In figure 2 the current through the capacitor C is

$$i_c = i_2 - i_1 \quad (3)$$

It provides the differential signal at the modulator input. A second function is the integration of the current signal. The voltage across the capacitor is given by equation 4:

$$v_c = \frac{1}{C} \int i_2 - i_1 dt \quad (4)$$

In this approach the capacitor voltage offers the signal for the clocked comparator.

In order to adjust the operating points for input current I_{in} as well as for the feedback current I_f a current subtractor is used as shown in figure 3.

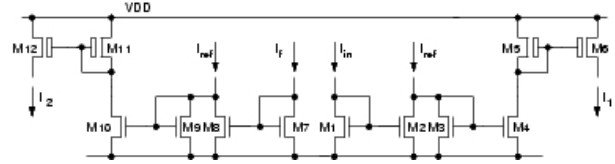


Fig. 3. Operating Point Adjustment for the currents

The subtraction is performed by the transistors M2/M3 for I_{in} and M8/M9 for I_f . With the current mirrors M5/M6 and M11/M12 the currents I_1 and I_2 are generated which offer two current sources. They provide the current signals for the integrator inputs in figure 2.

BIAS CURRENT GENERATION

A circuit architecture which is independent of the power supply voltage provides all biasing and reference currents of the circuit. This circuit is depicted in figure 4.

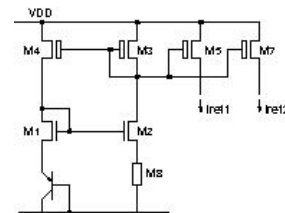


Fig. 4. Bias Current Generation

The resistor M8 adjusts the current, which is given by $I = V_{be} / R_8$. The currents of the current mirrors M3/M5 and M3/M7 are used for the reference currents in figure 3 and as well for the current based DAC as described in the following chapter.

CURRENT BASED DAC

The one bit DAC obtains the bitstream as its input signal as shown in figure 5. Two analog switches process the reference current I_{ref} depending the bitstream state. The output terminal

I_f conducts either the reference current or is being connected to ground. The inverter provides a negative representation of the bitstream for switch control.

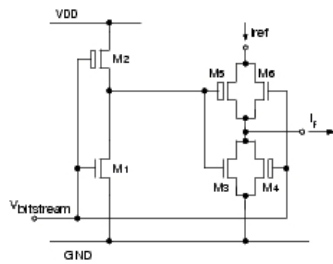


Fig. 5. Current Based DAC

CLOCKED COMPARATOR

A conventional comparator is used for converting the voltage signal v_{int} into the digital domain, as shown in figure 6.

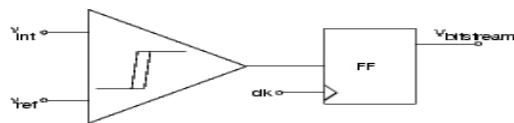


Fig. 6. Clocked Comparator

A small hysteresis of 1mV is adjusted by a built-in positive feedback stage. With a flip-flop the system clock is being fed in.

At the output of the flip-flop the system output of the modulator is offered - the bitstream signal.

SIMULATION RESULTS

For evaluation of the modulator function a sine wave signal is taken as the input current I_{in} . The simulation result is shown in figure 7.

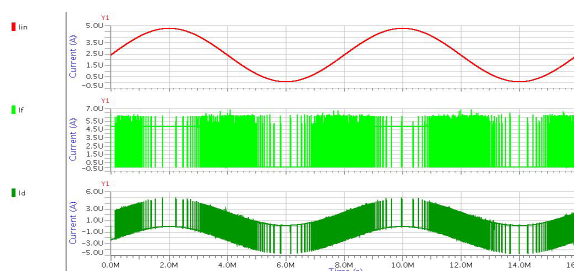


Fig. 7. Simulation Result

The upper waveform is the input current. The middle signal is the digital bitstream output signal and the lower waveform is the differential input signal of the current integrator.

Figure 8 shows the input signal on the upper axis and the quantization noise of the bitstream on the lower axis.

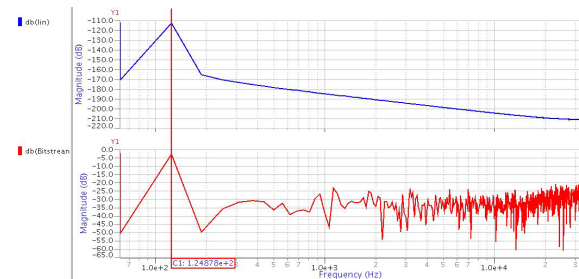


Fig. 8. Quantisation Noise

LAYOUT

The complete current-mode Delta-Sigma modulator has been realized in 0.35 μ CMOS technology and occupies a chip area of 0.015 mm². The layout is depicted in figure 9.

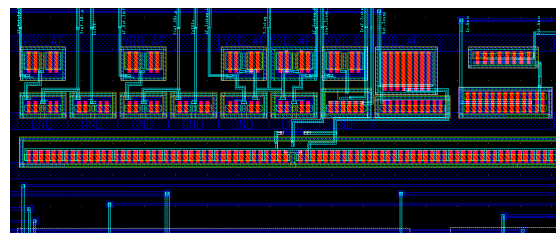


Fig. 9. Layout of the Current-Mode Delta-Sigma Modulators

CONCLUSION

In this paper a current-mode Delta-Sigma modulator is presented. The differential input signal processing as well as the signal integration are current based. Furthermore the DAC operates with a switched current which modulates the input current signal.

The integration circuit has been realized in 0.35 μ CMOS technology.

REFERENCE

- [1] E. I. El-Masry and J. W. Gates, "A Novel Continuous-Time Current-Mode Differentiator and Its Applications," IEEE Transc. on Circ. and Syst. II: Analog and Digital Signal Processing VOL. 43, No. 1, Jan 1996, pp. 56-59.
- [2] R. H. Zele, D. J. Allslot and T. S. Fiez, "Fully balanced CMOS current-mode circuits.", IEEE J. Solid-State Circuits, SC-28, pp. 569-575, May 1993.
- [3] S. Lee, R. Zele, D. Allstot, and G. Liang, "CMOS continuous-time current-mode filters for high-frequency applications.", IEEE J. Solid-State Circuits 28, pp. 323-329, March 1993.
- [4] Smith, Sterling L. et al., Low Voltage Integrators For High-Frequency CMOS Filters Using Current Mode Techniques, IEEE Transactions On Circuits And Systems II: Analog And Digital Signal Processing, Jan. 1996, vol. 43, No. 1.
- [5] A. Tang, F. Yuan, E. Law, "CMOS Current-Mode Active Transformer Sigma-Delta Modulators", Proc. IEEE Mid-West Symp. Circuits and Systems. pp. 625-628, Knoxville, TN., Aug. 2008.